

## SN74LS273N

### ■ Product Introduction

The SN74LS273N is an Octal D-type Positive-edge-triggered Flip-Flops(with Clear). Internal integration of 8 groups of D flip-flops triggered by rising edge, 8 groups share a zero-clearing input and a clock input.

### ■ Product Features

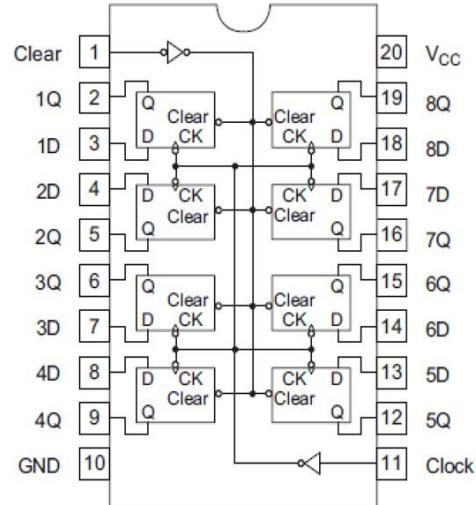
- Octal D-type Positive-edge-triggered Flip-Flops(with Clear)
- Fully compatible with TTL/DTL input and output logic level
- Package format: DIP20, SOP20

### ■ Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

### ■ Package and Pin Assignment

SOP20 or DIP20.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Clear	20	Supply VCC
2	Output 1Q	19	Output 8Q
3	Input 1D	18	Input 8D
4	Input 2D	17	Input 7D
5	Output 2Q	16	Output 7Q
6	Output 3Q	15	Output 6Q
7	Input 3D	14	Input 6D
8	Input 4D	13	Input 5D
9	Output 4Q	12	Output 5Q
10	Supply GND	11	Clock

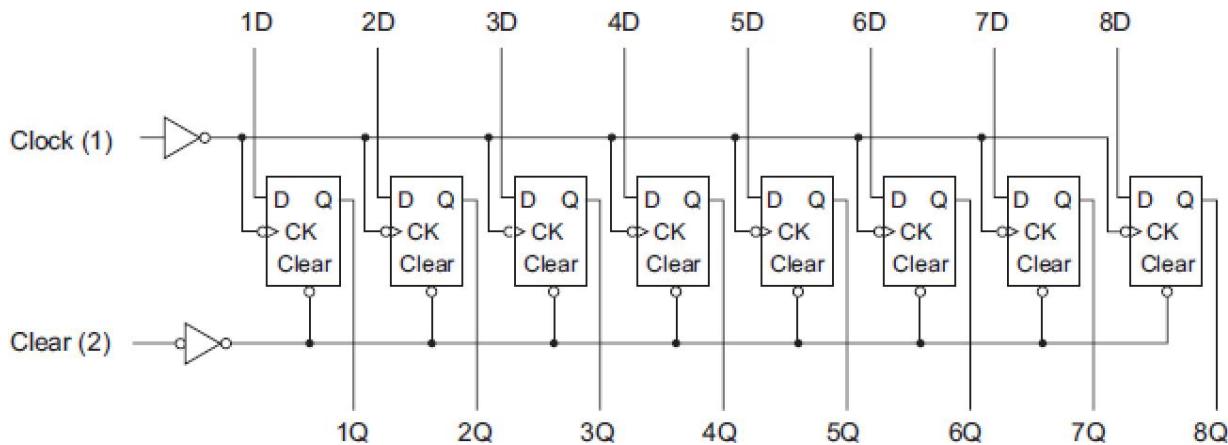


### ■ Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>I</sub>	7	V
Power dissipation	P <sub>D</sub>	500	mW
Operating temperature	T <sub>A</sub>	0-70	°C
Storage temperature	T <sub>S</sub>	-65-150	°C
Welding temperature	T <sub>W</sub>	260,10s	°C

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

## ■ Block Diagram



## ■ Function Table

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

Notes: H; high level, L; low level, X; irrelevant; ↑ ; transition from low to high level

Q<sub>0</sub>; level of Q before the indicated steady-state input conditions were established.

## ■ Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output current	I <sub>OH</sub>	—	—	-400	uA
	I <sub>OL</sub>	—	—	8	mA
Operating temperature	T <sub>opr</sub>	0	—	60	°C
Clock frequency	f <sub>clock</sub>	0	—	30	MHz
Clock pulse width	T <sub>W(CLK)</sub>	20	—	—	ns
Clear pulse width	T <sub>W(CLR)</sub>	20	—	—	ns
Data hold time	t <sub>h</sub>	5	—	—	ns
setup time	Data	t <sub>su</sub>	20	—	ns
	Clear (inactive-state)		25	—	ns

### Electrical Characteristics

( $T_A=25^\circ\text{C}$ , Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Input voltage	$V_{IH}$	2	—	—	V	
	$V_{IL}$	—	—	0.8	V	
Output voltage	$V_{OH}$	2.7	3.3	—	V	$I_{OH}=-400\mu\text{A}$
	$V_{OL}$	—	0.13	0.4	V	$I_{OL}=4\text{mA}$
		—	0.23	0.5		$I_{OL}=8\text{mA}$
Input current	$I_{IH}$	—	0.01	20	$\mu\text{A}$	$VCC=5.25\text{V}, V_I=2.7\text{V}$
	$I_{IL}$	—	0.25	-0.4	$\text{mA}$	$VCC=5.25\text{V}, V_I=0.4\text{V}$
	$I_I$	—	0.1	100	$\mu\text{A}$	$VCC=5.25\text{V}, V_I=7\text{V}$
Short-circuit output current *	$I_{OS}$	-20	-34	-100	$\text{mA}$	$VCC=5.25\text{V}$
Supply current**	$I_{CC}$	—	19	27	$\text{mA}$	$VCC=5.25\text{V}$
Input clamp voltage	$V_{IK}$	—	0.9	-1.5	V	$VCC=4.75\text{V}, I_I = -18\text{mA}$

Notes: \*only one output port is short circuited each time, and the short circuit time is not more than one second.

\*\* With all outputs open and 4.5 V applied to all data and clear inputs, ICC is measured after a momentary ground, then 4.5V is applied to clock.

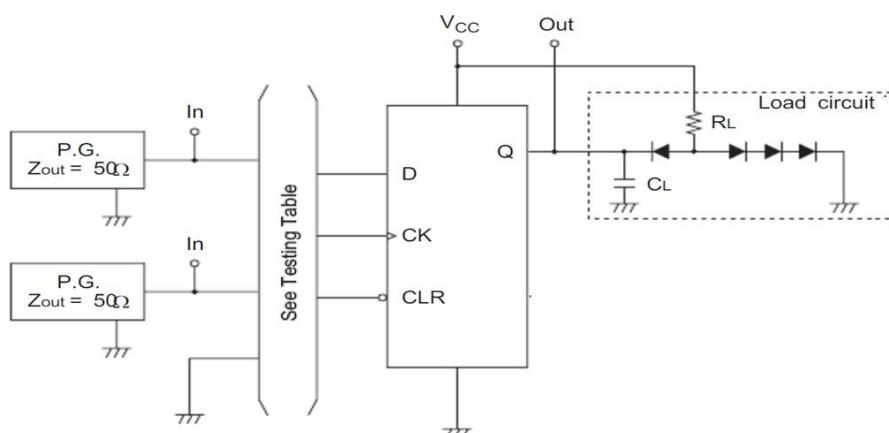
### Switching Characteristics

( $T_A=25^\circ\text{C}$ , Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Maximum clock frequency	$f_{max}$	0	25	—	MHz	$VCC=5\text{V}, CL=16\text{pF}$ $R_L=2\text{K}$
Propagation delay time Clock to Q	$t_{PLH}$	—	19	—	ns	
	$t_{PHL}$	—	15	—	ns	
Propagation delay time Clear to Q	$t_{PHL}$	—	25	—	ns	

### Testing Method

#### 1、Test Circuit



Notes:

A. Input signal pulse:  $f=1\text{MHz} D=50\% t_{TLH}=t_{THL}$  is less than 20ns. except for special regulations.

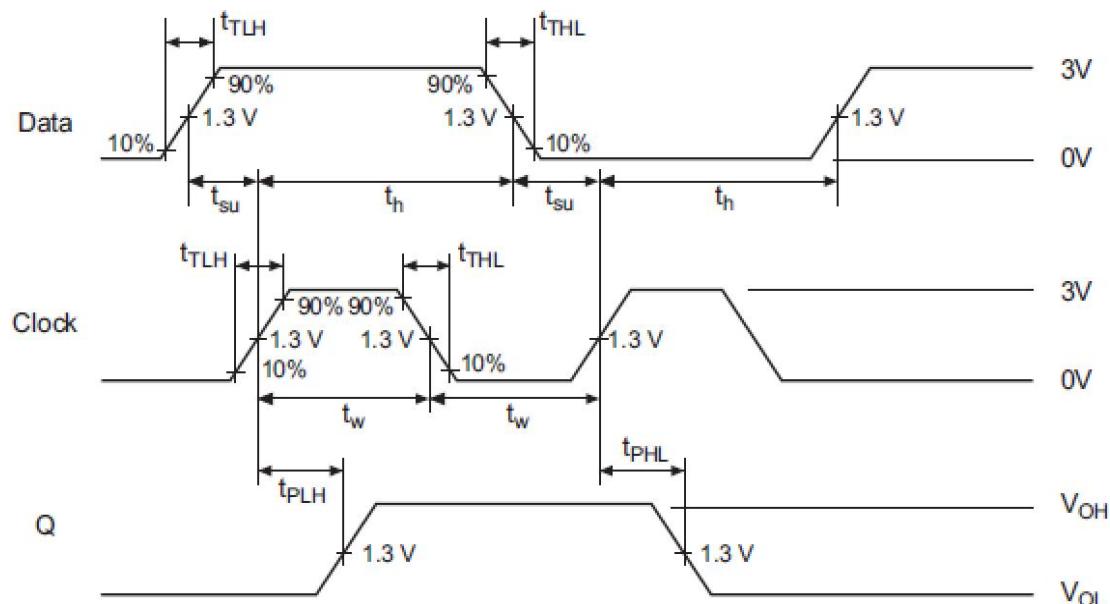
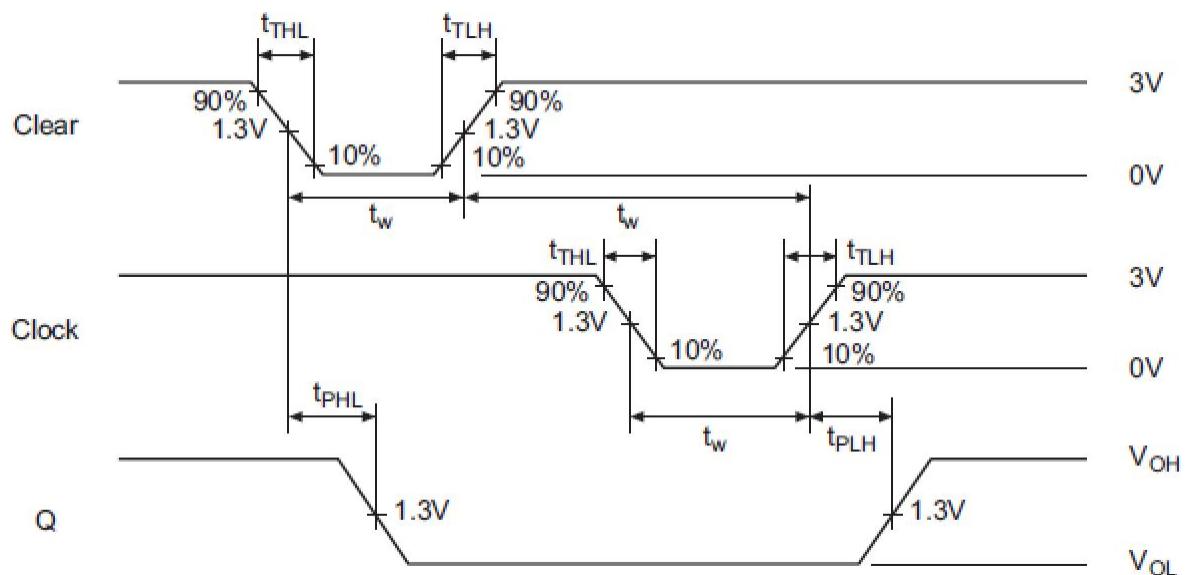
B. The CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.

C. All diode models are 1S2074 (H).

D. See Testing Table refers to the corresponding test items in the switch characteristic table.

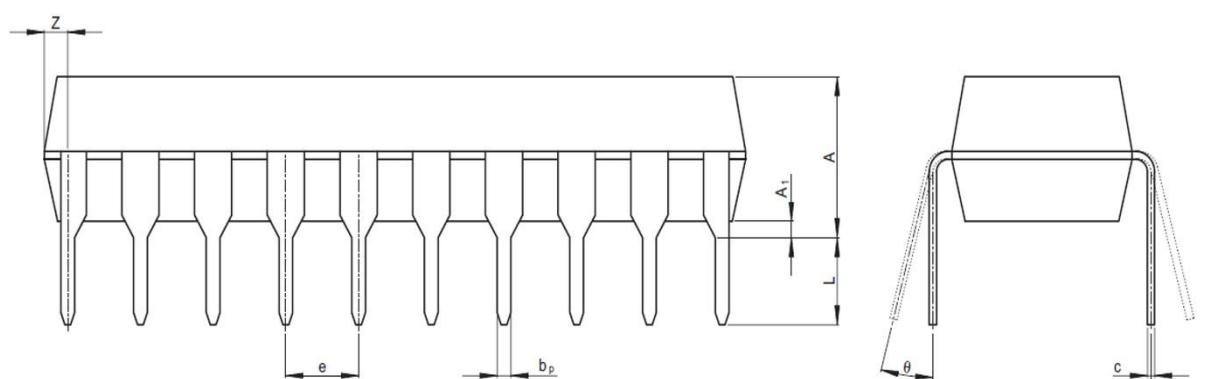
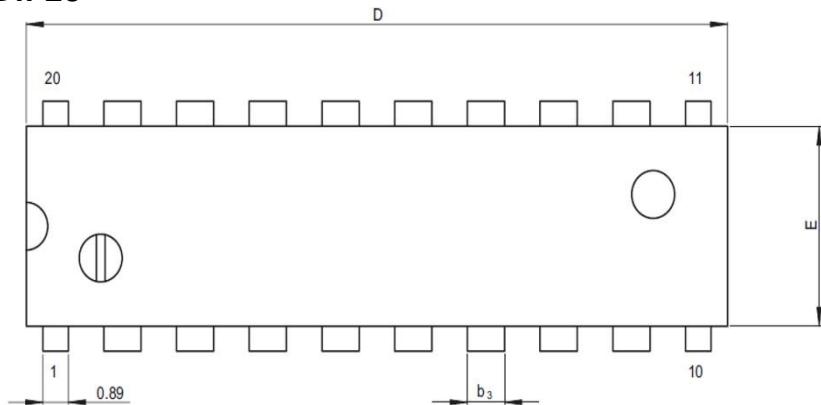
**2、Test item list**

Item	From input to output	Inputs			Outputs
		CLR	CK	D	
$f_{max}$	CK→Q	4.5 V	IN	IN	OUT
$t_{PLH}$	CK→Q	4.5 V	IN	IN	
$t_{PHL}$	CLR→Q	IN	IN	4.5 V	

**3、Waveform****4、Waveform**

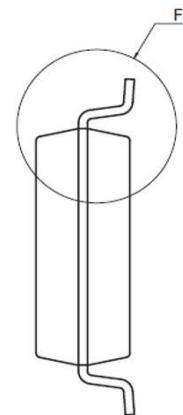
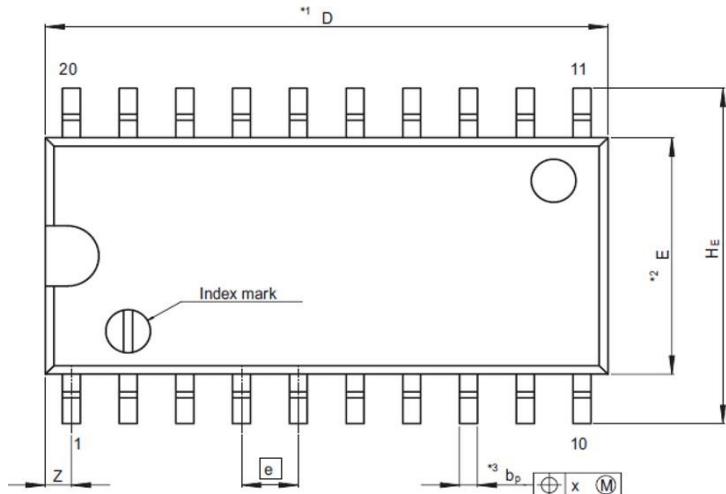
**■ Package Dimensions**

Unit : mm /inch

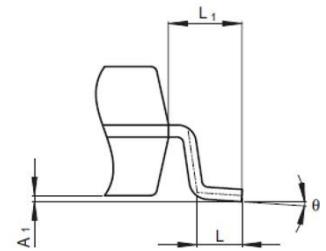
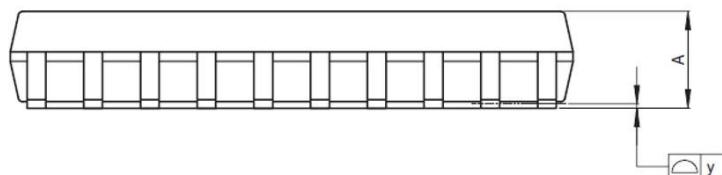
**DIP20**

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e <sub>1</sub>	—	7.62	—
D	—	24.50	25.40
E	—	6.30	7.00
A	—	—	5.08
A <sub>1</sub>	0.51	—	—
b <sub>P</sub>	0.40	0.48	0.56
b <sub>3</sub>	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.27
L	2.54	—	—

SOP20



Terminal cross section  
(Ni/Pd/Au plating)



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.60	13.0
E	—	5.50	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.00	0.10	0.20
A	—	—	2.20
b <sub>P</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	7.50	7.80	8.00
[e]	—	1.27	—
x	—	—	0.12
y	—	—	0.15
z	—	—	0.80
L	0.50	0.70	0.90
L <sub>1</sub>	—	1.15	—